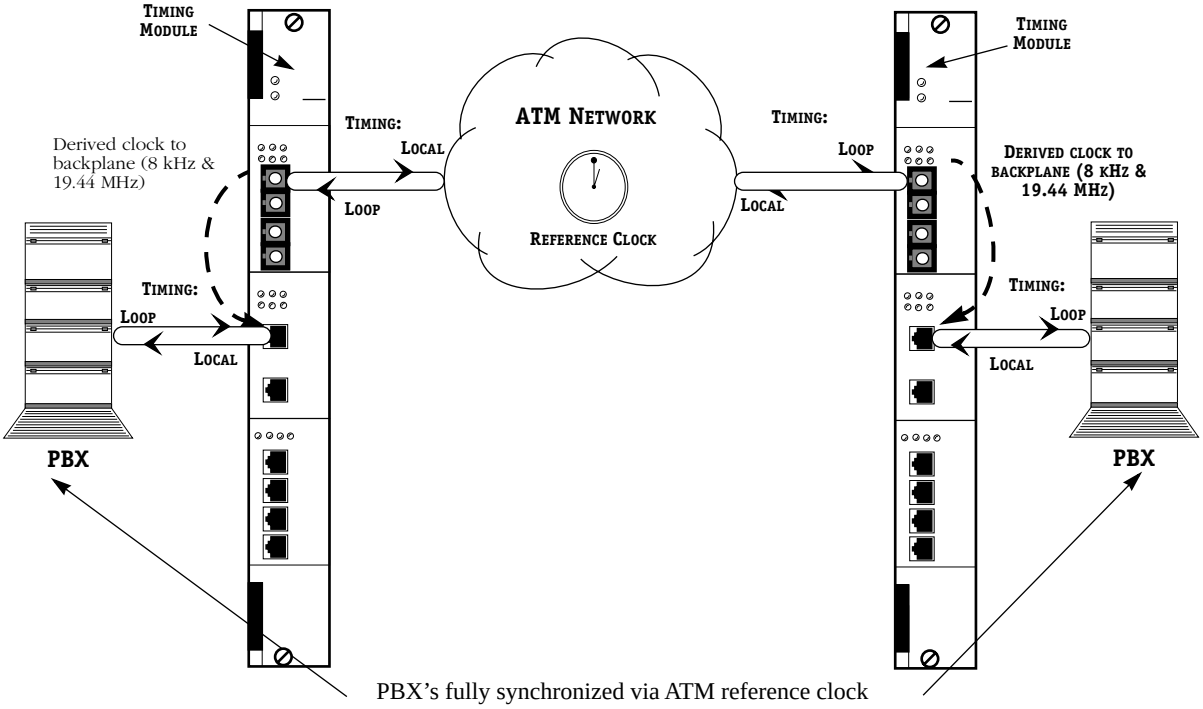
47 Clocking ATM Networks

Introduction

At first glance, it may seem odd to be speaking of clocking in conjunction with an asynchronous architecture such as ATM. However, in ATM, cells are transmitted asynchronously only at the ATM layer. It is still good design philosophy to synchronize the underlying physical layer — in cases where real-time data traffic exists (e.g., Circuit Emulation), it is a necessity. Network synchronization helps eliminate the major causes of data loss, namely phase separation (clock drift) and jitter. To maintain a cohesive network entity, a reference timing signal, or clock, must be distributed to all digital components in the network. This clock is generated and propagated at the physical layer.

The following illustration shows a typical ATM network configuration (implementing Cell-Switching Modules (CSMs)) and its associated timing architecture. The goal of CSM clocking is to enable edge devices (in this example, PBXs) at opposite ends of an ATM-centric network to be tightly synchronized to one another via a single, primary clock source.



Clocking Sources in a Typical ATM Network Configuration

ATM Data Traffic

Having an accurate, reliable reference clock is especially important in system architectures that require Constant Bit Rate (CBR) data traffic, such as uncompressed voice and video. CBR provides a guaranteed bandwidth, so that data loss is kept to a strict minimum. This is necessary because these data types are highly sensitive to data loss. However, other less timing-sensitive data traffic types can still realize benefits from a single-reference clock design.

Selecting Clocking Sources

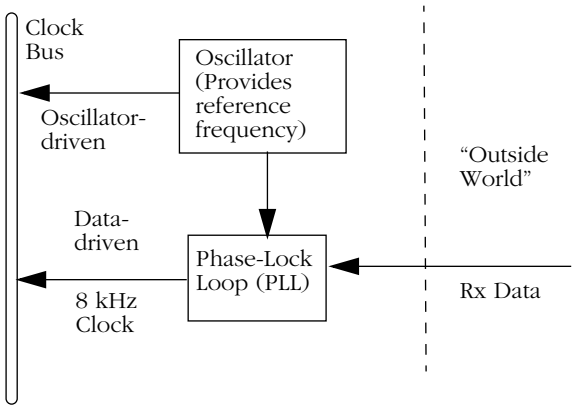
The flexibility designed into the OmniSwitch allows it to implement a variety of possible reference clocking schemes. The design also provides for alternate clocking sources in the event of a primary source failure.

You configure clocking at two levels, port level and bus level. Port-level configuration specifies the source of the transmit clock driving the port. Bus-level clock configuration specifies the clock source to the backplane of the system.

Configuring Transmit Clocking (Port-Level Clocking)

In port-level clocking, you are specifying a clock source for the port to "use" (i.e., drive its transmit data). All ports on all modules use either 8 kHz or 19.44 MHz reference timing. A different clock source can be specified for every port in the system.

When the clock comes from the receive data, the term "derive" means that the clocking signal is separated from the receive data by a Phase-Lock Loop, then sent to a bus on the backplane. When the clock comes from an onboard oscillator, the oscillator provides clocking directly to the bus.



Modules can derive reference timing from either:

- the receive data stream (data-driven clocking)
- in some cases, from an onboard oscillator (oscillator-driven clocking)
- an optionally-installed Stratum 3 hardware clocking module.

Modules that Require 8 kHz Timing

The following types of modules use an 8 kHz clock for driving their data:

- E1/T1
- DS1
- E3
- ATM-25
- CE-E1/T1

Modules that use an 8 kHz clock can derive their timing from:

- The locally-generated clock from the 19.44 MHz onboard oscillator on the CSM module (divided down to 8 kHz by the PLL module),
- The receive data, or
- The optionally-installed X-Cell Clocking Module (CSM-AB-CM; for more information on this module, see Chapter 41, "Cell Switching Modules (CSMs).")

Modules that Require 19.44 MHz Timing

The following types of modules use a 19.44 MHz clock for driving their data:

- OC3
- OC12
- CE-E1/T1

Modules that use a 19.44 MHz clock can derive their timing from:

- The locally-generated clock from the 19.44 MHz onboard oscillator on the CSM module,
- The receive data, or
- The optionally-installed X-Cell Clocking Module (CSM-AB-CM)

Timing Considerations for DS3/E3 and PLCP

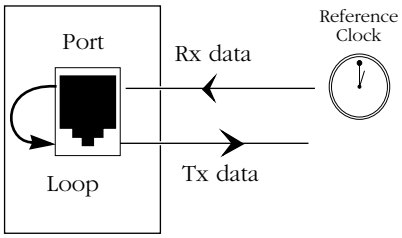
The DS3/E3 data format may be managed by the Physical Layer Convergence Protocol (PLCP), which incorporates its own clocking information. While PLCP is an optional method for providing clocking, it is required for data requiring synchronization of clocking. PLCP provides services to map the ATM cells into the DS3 frame structure. Timing data for an 8 kHz clock is encoded into the PLCP data, and is derived independently from the carrier frequency. The DS3 and E3 modules are capable of utilizing this timing data for both source clocking of receive data to the bus and as a reference clock for transmit data at 8 kHz.

Timing Modes

Two transmit timing mode options are available: loop timing and local timing. For details on setting the timing mode, see *Configuring Clocking* on page 47-10.

Loop Timing

Loop timing is typically implemented with public network connections. In loop timing, the reference clock is derived from the receive data, then fed back out with the transmit data.



Local Timing

For local timing mode, you set which source a port is to use to drive its transmit data. The options are:

- The local oscillator. Using the local oscillator (located on the CSM module) will provide the backplane with a Stratum 4-level clock.
- The bus (backplane). You can select either the 8 kHz or 19 MHz bus, depending upon the port type. Select this option if you are planning to provide a single reference clock across the network.
- The optionally-installed X-Cell Clocking Module (CSM-AB-CM). This module provides a Stratum 3-level clock to the 8 kHz and 19.44 MHz buses.

Bus-Level Clocking

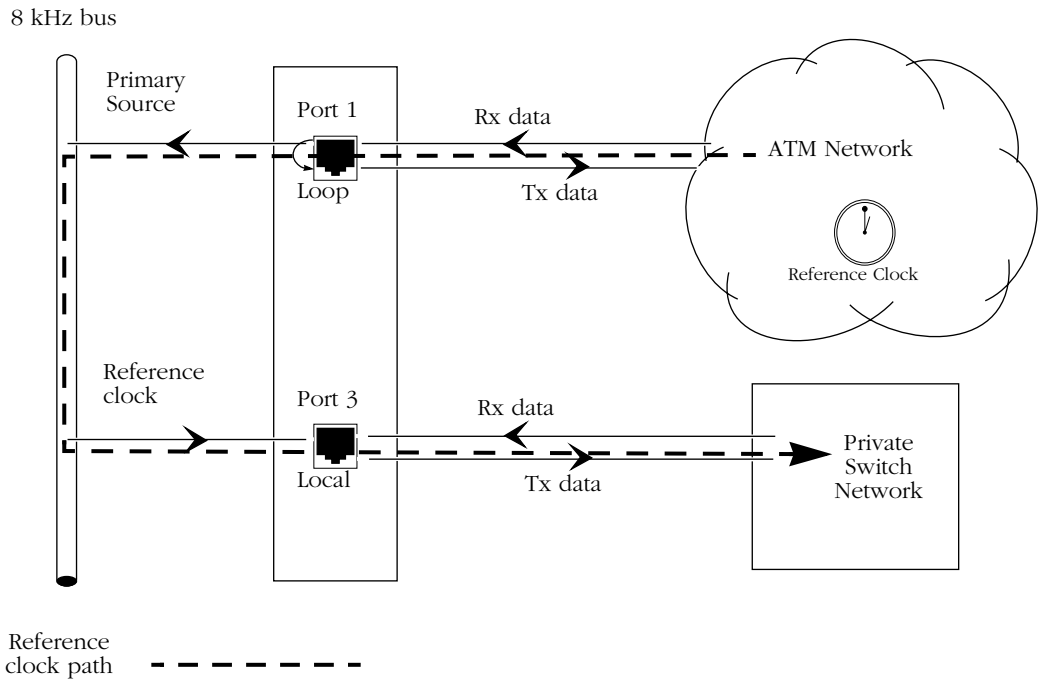
In bus-level clocking, you are specifying whether the clock that drives the bus on the backplane comes from a source within the switch, or from an external source. Some examples of external sources are:

- Commercial ATM services
- Public network T1 lines
- PBXs
- Other switching modules

Bus Lines

There are two clocking lines on the backplane; an 8 kHz clock and a 19.44 MHz clock.

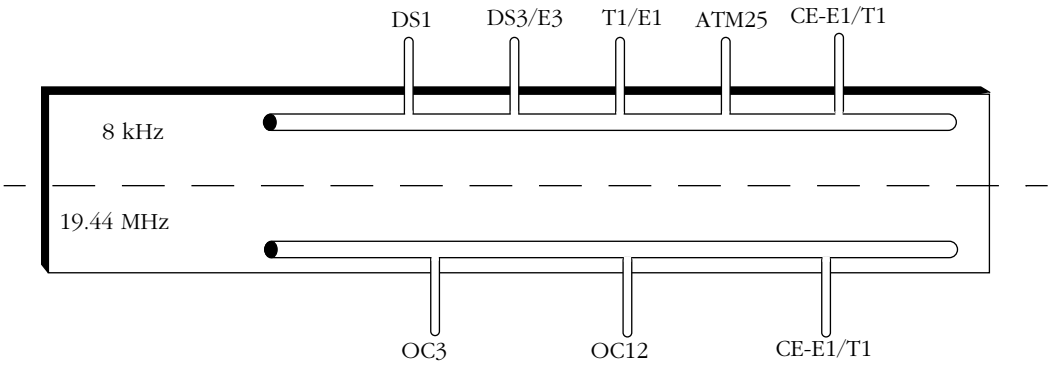
The following illustration shows an example of ports on a switch deriving their timing from a commercial ATM provider via loop timing, then passing that reference clock on through another port to synchronize a private network (local timing).



Synchronizing a Private Network Through Derived Timing

Clocking Summary

The following figure is a representation of the backplane clock sources and the CSM modules they support.



Backplane Clock Sources

The following tables summarize the port types and their reference clocking options:

In this table, the oscillator associated with the port is driving the bus.

Board	Line Clock (MBPS)	Rx Data Recovered (8 kHz)	Rx PLCP (8 kHz)	8 kHz Oscillator	Rx Data Recovered (19.44 MHz)	19.44 MHz Oscillator
OC12-2	622	Y	N/A	N	Y	Y
OC3-2, -8	155	Y	N/A	N	Y	Y
DS3-2	45	Y	Y	Y	N	Y
E3-2	34	Y	Y	Y	N	Y
DS1-4	1.544	Y	N/A	Y	N	Y
E1-4	2.048	Y	N/A	Y	N	Y
ATM25-12, -24	25.6	Y	N/A	N	N	N
CE-T1/E1	1.544/2.048	Y	N/A	N	Y	Y

This table lists which buses can drive the ports associated with the particular board.

Board	Line Clock (MBPS)	Tx Regenerated Line Clock from 8 kHz	Tx PLCP 8 kHz from 8 kHz	Tx Regenerated Line Clock 19.44 MHz)	Tx PLCP 8 kHz from 19.44 MHz
OC12-2	622	N	N/A	Y	N/A
OC3-2, -8	155	N	N/A	Y	N/A
DS3-2	45	N	Y	N	N
E3-2	34	N	Y	N	N
DS1-4	1.544	Y	N/A	N	N/A
E1-4	2.048	Y	N/A	N	N/A
CE-T1-4	1.544	Y	N/A	Y	N/A
CE-E1-4		Y	N/A	Y	N/A
ATM25-12, -24	25.6	Y	N/A	N	N/A

Viewing/Configuring Clocking

The following commands are the commands to configure clocking and to view the clocking configuration. They are listed in the **Interface/ATM** menu.

- Use the **vap** command to view configuration information for all CSM ports, including the current clocking status. This command provides information on the timing mode and source for each port. (See *Viewing ATM Port Configurations* in Chapter 35 "Managing ATM Access Modules")
- Use the **map** command to set the timing mode (either loop or local) for ATM ports only. (See *Modifying the Transmit Clocking Source* on page 47-12.)
- Use the **vclk** command to view clocking status for configured CSM ports only. (See *Viewing Configured Ports* on page 47-8.)
- Use the **vclka** command to view clocking information on all CSM ports. (See *Viewing Clocking on All Ports* on page 47-9.)
- Use the **mclk** command to alter clock configuration settings for CSM ports. (See *Configuring Clocking* on page 47-10.)
- Use the **mcst** command to set the amount of time the backup clock source waits before it returns timing control back to the recovered primary clock source. (See *Modifying the Clock Switching Time (CSM Ports)* on page 47-11.)

Viewing the Clocking Configuration

Two commands, **vclk** and **vclka**, enable you to view the clocking sources of the buses at the backplane, as well as the clocking source for the port(s). The **vap** command enables you to view the configured transmit clocking source for the switch.

Viewing Configured Ports

The **vclk** command is listed in the Interface/ATM menu. It returns clocking information on only those CSM ports that have been configured as clock sources to the backplane.

To view all configured ports, type **vclk** at the prompt. The following screen is a sample a switch that has had only the primary clock source defined:

```
                                Clock Source
                                ------------

                    Timing      Configured  Current
Slot  Port Mode     Source      Source
==== ==== ========== ========== ==========
5     1    Local     19.44 MHz  19.44 MHz

Reference Source  Primary  Secondary   Tertiary   Current
================ ======= =========== ======== =========
 8 kHz           5/1      None        None     Primary
19.44 MHz        4/1      None        None     Primary
```

Note that only port 5/1 is displayed. If secondary and tertiary ports had been defined as clocking sources, they, too, would have been displayed. The following information is displayed for the configured port(s):

Slot/Port. Indicates the CSM module and the port number for which statistical information is provided. Each row in the table gives information for a single CSM port.

Timing Mode. Can be set to either **Loop** or **Local**. If the port is set to **Loop**, it is deriving its clocking directly from the receive data, not from the bus. If the port is set to **Local**, it is deriving its clocking from the bus.

Configured Source. Refers to the bus from which the port is configured to be receiving its reference clock. Options are 8 kHz and 19.44 MHz.

Current Source. Refers to the bus from which the port is currently receiving its reference clock. Options are 8 kHz and 19.44 MHz.

Note

If Configured Source and Current Source are different, it is a probable indicator that the port's configured source has failed.

The second table shows what ports (if any) are configured as the primary, secondary, and tertiary reference clocks. The table also shows what level is currently active.

Viewing Clocking on All Ports

The **vclka** command is listed in the Interface/ATM menu. It returns information on the clocking source for all CSM ports on the system. The following screen is a sample of the output from the **vclka** command:

```
                                Clock Source
                                ------------

                    Timing      Configured      Current
Slot  Port          Mode        Source          Source
========  ========  ======      ============    ============
4         1         Local       Oscillator      Oscillator
4         2         Local       Oscillator      Oscillator
5         1         Local       19.44 MHz       19.44 MHz
5         2         Local       Oscillator      Oscillator
5         3         Local       Oscillator      Oscillator
5         4         Local       Oscillator      Oscillator
5         5         Local       Oscillator      Oscillator
5         6         Local       Oscillator      Oscillator
5         7         Local       Oscillator      Oscillator
5         8         Local       Oscillator      Oscillator

Reference Source    Primary     Secondary       Tertiary    Current
================    =======     ==========      ========    =========
 8 KHz              5/1         None            None        Primary
19.44 MHz           4/1         None            None        Primary
```

Field Descriptions

The following section describes the fields and their optional values.

Slot/Port. The slot within the chassis and the port on that module for which information will be displayed. This command displays information for a single port in one row.

Timing Mode. This field has two options: **Loop** and **Local**. **Loop**, means the port is deriving its clocking directly from the receive data. **Local**, means the port is deriving its clocking from the bus.

Configured Source. This field will indicate that the current source for the port is either its local oscillator (the default setting), or one of the buses.

Current Source. This field indicates that the configured source for the port is either its local oscillator (the default setting), or one of the buses.

Note

If Configured Source and Current Source are different, it is a probable indicator that the port's configured source has failed.

The second table provides a summary of what ports (if any) are providing the primary, secondary, and tertiary clock source to each of the bus lines at the backplane.

Configuring Clocking

The **mclk** command enables you to modify the clocking sources to the backplane. The **mcst** command enables you to set the amount of delay before the backup clock source returns control to the recovered primary clocking source. The **map** command enables you to specify the transmit clocking source(s) for the switch.

Modifying the Clocking Configuration (CSM Ports)

To alter the clocking configuration settings for CSM ports, use the **mclk** command. **mclk** is listed in the Interface/ATM menu. To view the format and valid ranges for **mclk**, type the command without any parameters, then press **<return>**, as shown below:

```
mclk <return>
```

A screen similar to that shown below is displayed:

```
/Interface/atm% map 2/1

Usage:  mclk bus level source
Valid ranges:
 bus:    8k OR 19m for OC3 and OC12
          8k for DS3/E3, ATM25, T1E1, IMA, and T1E1-CE
level:  p for Primary, s for Secondary, OR t for Tertiary
source:  slot/port OR slot/port osc OR none
```

To modify a clocking configuration, enter the command in the following format:

```
mclk <bus> <backup level> <slot>/<port> (osc)
```

Field Descriptions

The following section describes the valid options to enter and their associated parameters.

bus: Enter the bus to which you want to provide the source clock. Available options are **8k** (for the 8kHz bus) and **19m** (for the 19.44 MHz bus). For OC3, OC12 or CE-E1/T1 ports, you can set the clock to either 8k or 19m. For all other port types, the clock must be set to 8k.

level: Set to **p** (primary), **s** (secondary), or **t** (tertiary). For more information on backup levels, see *Backup Design* on page 47-14.

Note

If you define a secondary clocking source without defining a primary source, the switch will automatically derive its clocking from the secondary source. Similarly, if you define a tertiary source only, the system will use that source.

source. The slot within the chassis and the port on that module that will drive the bus. Available options are: **<slot>/<port>**, **<slot>/<port> osc**, and **none**. Include the **osc** option if you want to specify the onboard oscillator as the clock source.

If you have the optional hardware clocking module installed in your switch, and you select the slot/port that corresponds to the module, its module's external T1/E1 port will drive the backplane. If you add the **osc** option, the module's onboard Stratum 3 clock will drive the backplane.

Select the **none** option if this port will not be used as a source of clocking. The **none** option may also be used to deconfigure a port that was previously configured as a source to the backplane.

Examples

For example, to specify slot 5, port 1 (**5/1**) as the primary (**p**) source to drive the 8 kHz bus (**8k**) at the backplane, enter:

```
mclk 8k p 5/1
```

In this example, slot 4 is occupied by a CSM. The following command specifies slot 4, port 1 (**4/1**) as the secondary (**s**) source to drive the 19 MHz bus (**19m**) at the backplane, and the onboard oscillator as the secondary (backup) clock source:

```
mclk 19m s 4/1 osc
```

For this example, the hardware clocking module is installed in slot/port 6/1. The following command specifies the clocking module as the primary source to drive bus 8k at the backplane, using the onboard Stratum 3 clock.

```
mclk 8k p 6/1 osc
```

Modifying the Clock Switching Time (CSM Ports)

The **mcst** command provides an additional configuration option for the clock module. The setting for this command comes into play in the event of the loss of the primary clocking source. Should the primary clocking source go down, then subsequently come up again, the switch will wait the specified amount of time (in seconds) before switching back from the backup clocking source to the restored primary clocking source. The purpose of this delay is to avoid having the switch repeatedly switching between the primary and backup clocking sources in the event of an unstable or unreliable primary clocking source.

This command is listed in the Interface/ATM menu. The only parameter that is set on the **mcst** command is the amount of switchover delay. This delay can be set anywhere in the range of 1 to 10000 seconds. The delay applies to the entire clocking system. The default value is 5 seconds.

To use the **mcst** command, enter **mcst**, followed by the amount of delay. For example, to set the switchover delay to 10 seconds, you would enter:

```
mcst 10
```

A screen similar to the following now displays, showing both the current configured clock sources and switchover time:

```
                        Clock Source
                        ------------

            Timing      Configured  Current
Slot  Port  Mode        Source      Source
====  ====  ==========  ==========  ==========
5     1     Local       19.44 MHz   19.44 MHz

Reference Source  Primary  Secondary   Tertiary   Current
================  =======  ==========  ========   =========
 8 kHz            5/1      None        None       Primary
19.44 MHz         4/1      None        None       Primary

Clock switching time (seconds)
==========================
10
```

See *Viewing Clocking on All Ports* on page 47-9 for more information on the parameters displayed by the **mcst** command.

Modifying the Transmit Clocking Source

To modify the transmit clocking source, use the Timing Mode option (parameter 9) of the **map** command. The **map** command is listed in the Interface/ATM menu. The valid options for the Timing Mode option are **Loop (1)** and **Local (2)**.

If the Local option of the Timing Mode parameter is selected, a subparameter called Local Source (parameter 90) must be set. The valid options are **Osc (1)** (for the onboard oscillator, or in the case where the port corresponds to the optional hardware clocking module, the Stratum 3 clock), or **Bus (2)** (meaning the clock is derived from either the 8 kHz or 19.44 MHz backplane, depending upon the type of module being configured and its timing requirements).

To use the **map** command, enter **map**, followed by **<slot>/<port>**. For example, to modify the first port on slot two, enter:

```
map 2/1
```

A screen similar to the following displays:

```
/Interface/atm% map 2/1

  Slot 2 Port 1 Configuration

1)      Description (30 chars max)                    : CSM PORT
2)      ATM Address (40 hex-chars)                    :
00000000000000000000000000000000000000000000
3)      Max VPI bits (1..12)                          : 2
4)      Max VCI bits (1..12)                          : 10
5)      I/F Type {Pub UNI (1), Pri UNI (2),
PNNI (3), IISP user (4), IISP netw (5): Private
6)      Phy Protocol {SONET (1), SDH (2)              : SONET
7)      Signaling Ver {3.0 (1), 3.1 (2)               : 3.0
8)      ILMI Enable {False (1), True (2) }            : Enable
9)      Timing Mode {Local (1), Loop (2) }            : Local
   90)     Local Source {Osc(1), Bus(2) }             : Bus


Enter (option=value/save/cancel) :
```

To set or change the Timing Mode for the selected port, enter 9={1/2}. '1' sets the port to **Loop** timing; '2' sets the port to **Local** timing. For example:

```
9= 1
```

Sets port 2/1 to Local timing. To save the new configuration, type **save**, then press **<Enter>**. For more detailed information on Local vs Loop timing, see *Configuring Transmit Clocking (Port-Level Clocking)* on page 47-2.

If you set the Timing Mode to Local, you must next set the subparameter called Local Source (subparameter 90). The options are **Osc (1)** and **Bus (2)** . **1** sets the port's clocking source to the onboard oscillator, or to the Stratum 3 clock, if the port you selected corresponds to the hardware clocking module. **2** sets the clocking source to the bus (the system will automatically select either the 8 kHz or 19.44 MHz bus, as required by the port being configured).

See Chapter 42, "Managing Cell Switching Modules (CSMs), for more information on the **map** command.

Modifying the Transmit Clocking Source (T1/E1 Ports)

For most CSM modules, when the timing mode is set to **Local**, the software automatically selects the bus with the appropriate clock for that module (e.g., 8k for an ATM-25 port; 19M for an OC3 port). Since T1/E1 ports can be clocked off of either bus, T1/E1 ports are user-configurable for that option. Suboption 90, **Local Source**, provides three options: **Osc(1), 8KBus(2),** and **19MBus (3).** When you invoke the **map** command for a T1 or E1 port, a screen similar to that shown below is displayed:

```
/Interface/atm% map 2/1

  Slot 2 Port 1 Configuration

1)      Description (30 chars max)                    : CSM PORT
2)      ATM Address (40 hex-chars)                    :
00000000000000000000000000000000000000000000
3)      Max VPI bits (1..12)                          : 2
4)      Max VCI bits (1..12)                          : 9
9)      Timing Mode {Local (1), Loop (2) }            : Local
   90)      Local Source {Osc(1), 8KBus(2)
            19MBus (3) }                              : 8KBus


Enter (option=value/save/cancel) :
```

If you set Timing Mode (Option 9) to the **Local** option, you must specify which Local Source you want to use: the onboard oscillator (**Osc(1)**), the 8 kHz bus (**8KBus(2)**), or the 19 MHz bus (**19MBus (3)**).

See Chapter 42, "Managing Cell Switching Modules (CSMs), for more information on the **map** command.

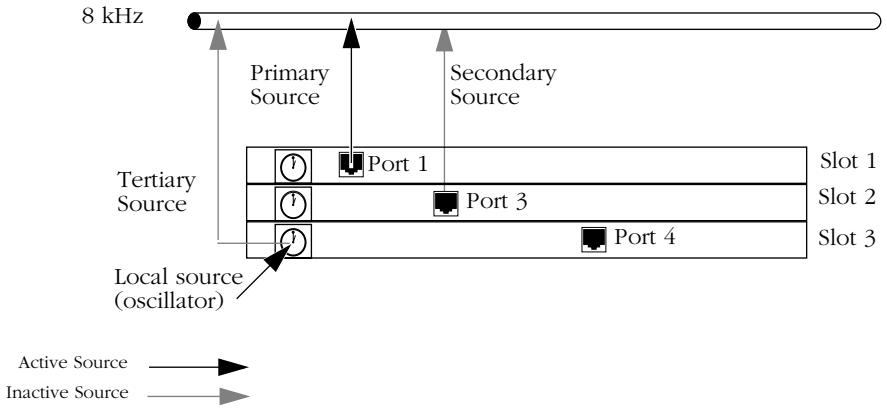
Clock Backup

The system software is capable of handling clock backup tasks when communication over a port fails in the system. To set backup levels for one or more ports, use the **mclk** command (see *Configuring Clocking* on page 47-10).

Backup Design

You can configure the system to provide up to three levels of clock backup in the event of port failure by configuring primary, secondary, and tertiary sources to the backplane reference source (8k or 19m). By default, the local oscillator drives the ports in the system. If the primary source fails, the system will automatically switch to the secondary source to drive the reference source. If the primary source should come back up, it will take over and drive the backplane. If both the primary and secondary sources fail, the system will switch to the tertiary backup (usually a local oscillator). If all three sources fail, the system will switch to a local oscillator for local timing. If any of the failed sources comes back up, the tertiary source hands the clock back to it. If no source is driving the backplane, the system will switch the ports to their local oscillator.

In the example below, Slot 1/Port 1 is configured as the primary source. It is driving the 8 kHz bus (8k) at the backplane. Slot2/Port 3 is configured as the backup to Primary Source, and is referred to as the secondary source. If the primary source should fail, the system will automatically switch to the secondary source, which will immediately begin driving bus 8k.



Sample Backup Configuration

If the secondary source should subsequently fail, and a tertiary source has been configured (in this example, the local oscillator on slot 3), the system would switch to the oscillator to drive the backplane. Thus, the onboard oscillator would become the tertiary source. If the tertiary source were not configured, the ports relying on the 8k clock bus as a reference source would be switched to their local onboard oscillators.

If at any time port 1 or 3 should come back up, it will resume its responsibility for driving bus 8k (after the configured Clock Switching Time (**mcst**) has elapsed).